

**Features**

288-pin JEDEC-compliant DIMM, 133.35 mm wide by 31.25 mm high

Operating Voltage: VDD/VDDQ = 1.2V (1.14V to 1.26V)

VPP = 2.5V (2.375V to 2.75V)

VDDSPD = 2.25V to 2.75V

I/O Type: 1.2 V signaling

On-board I<sup>2</sup>C temperature sensor with integrated Serial Presence-Detect (SPD) EEPROM

Data Transfer Rate: 17.0 Gigabytes/sec

Data Bursts: 8 and burst chop 4 mode

ZQ Calibration for Output Driver and On-Die Termination (ODT)

Programmable ODT / Dynamic ODT during Writes

Programmable CAS Latency: 9, 10, 11, 12, 13, 14, 15 and 16

Bi-directional Differential Data Strobe signals

Per DRAM Addressability is supported

Write CRC is supported at all speed grades

DBI (Data Bus Inversion) is supported(x8 only)

CA parity (Command/Address Parity) mode is supported

Supports ECC error correction and detection

16 internal banks

SDRAM Addressing (Row/Col/BG/BA): 15/10/2/2

Fully RoHS Compliant

**Identification**

DTM68104B 1Gx64

8G 2Rx8 PC4-2133P-UB0-10

**Performance range**

Clock / Module Speed / CL-t<sub>RCD</sub>-t<sub>RP</sub>

1067 MHz / PC4-2133 / 16-16-16

1067MHz / PC4-2133 / 15-15-15

933 Hz / PC4-1866 / 14-14-14

933 Hz / PC4-1866 / 13-13-13

800 Hz / PC4-1600 / 12-12-12

800 Hz / PC4-1600 / 11-11-11

667 MHz / PC4-1600 / 10-10-10

667 MHz / PC4-1600 / 9-9-9

**Description**

DTM68104B is an unbuffered 1Gx64 memory module, which conforms to JEDEC's DDR4-2133, PC4-2133 standard. The assembly is Dual-Rank. Each rank is comprised of eight Micron 512Mx8 DDR4-2133 SDRAMs. One 2K-bit EEPROM is used for Serial Presence Detect.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals in a Fly-by topology. A thermal sensor accurately monitors the DIMM module and can prevent exceeding the maximum operating temperature of 95C.

### Speed Bin Table

Speed Bin			DDR4-2133P		DDR4-2133R		Unit	NOTE
CL-nRCD-nRP			15-15-15		16-16-16			
Parameter		Symbol	min	max	min	max		
Internal read command to first data		tAA	14.06 <sup>14</sup> (13.50) <sup>5,12</sup>	18.00	15.00	18.00	ns	
Internal read command to first data with read DBI enabled		tAA_DBI	TBD	TBD	TBD	TBD	ns	
ACT to internal read or write delay time		tRCD	14.06 (13.50) <sup>5,12</sup>	-	15.00	-	ns	
PRE command period		tRP	14.06 (13.50) <sup>5,12</sup>	-	15.00	-	ns	
ACT to PRE command period		tRAS	33	9 x tREFI	33	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	47.06 (46.50) <sup>5,12</sup>	-	48.00	-	ns	
	Normal	Read DBI						
CWL = 9	CL = 9	CL = 11 (Optional) <sup>5</sup>	tCK(AVG)	1.5	1.6	Reserved		1,2,3,4 ,11,14
			tCK(AVG)	(Optional) <sup>5,12</sup>				
	CL = 10	CL = 12	tCK(AVG)	Reserved		1.5	1.6	ns 1,2,3,1 1
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	Reserved		1,2,3,4 ,7
			tCK(AVG)	(Optional)5,12				
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	1.25	<1.5	ns 1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	Reserved		1,2,3,4 ,7
			tCK(AVG)	(Optional) <sup>5,12</sup>				
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	1.071	<1.25	ns 1,2,3,7
CWL = 11,14	CL = 14	CL = TBD	tCK(AVG)	Reserved		Reserved		ns 1,2,3,4
	CL = 15	CL = TBD	tCK(AVG)	0.938	<1.071	Reserved		ns 1,2,3,4
	CL = 16	CL = TBD	tCK(AVG)	0.938	<1.071	0.938	<1.071	ns 1,2,3
Supported CL Settings			(9),(11),12,(13),14,15, 16		10,12,14,16		nCK	13,14
Supported CL Settings with read DBI			TBD		TBD		nCK	
Supported CWL Settings			9,10,11,12,14		9,10,11,12,14		nCK	

**Speed Bin Table Notes:****Absolute Specification**

- VDDQ = VDD = 1.20V +/- 0.06 V

- VPP = 2.5V +0.25/-0.125 V

- The values defined with above-mentioned table are DLL ON case.

- DDR4-1600, 1866, 2133 and 2400 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.

2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL – all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.

3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is tCK(avg). MAX corresponding to CL SELECTED.

4. 'Reserved' settings are not allowed. User must program a different value.

5. 'Optional' settings allow certain devices in the industry to support this setting however it is not a mandatory feature.

Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.

6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

9. Reserved for DDR4-2666 speed bin.

10. Reserved for DDR4-3200 speed bin.

11. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.

12. For devices supporting optional down binning to CL=9, CL=11 and CL=13, tAA/tRCD/tRPmin must be 13.5ns or lower. SPD settings must be programmed to match. For example, DDR4-1600K devices supporting down binning to 1333MT/s should program 13.5ns in SPD bytes for tAAmin(Byte 24), tRCDmin (Byte 25), and tRPmin (Byte 26). DDR4-1866M devices supporting down binning to 1333MT/s or DDR4-1600K should program 13.5ns in SPD bytes for tAAmin (Byte 24), tRCDmin (Byte 25), and tRPmin (Byte 26). DDR4-2133P devices supporting down binning to 1333MT/s or DDR4-1600K or DDR4-1866M should program 13.5ns in SPD bytes for tAAmin (Byte 24), tRCDmin (Byte 25), and tRPmin (Byte 26). tRCmin (Byte 27, 29) also should be programmed accordingly. For example, 48.5ns (tRASmin + tRPmin = 35ns + 13.5ns) is set to supporting optional down binning CL=9 and CL=11.

13. CL number in parentheses, it means that these numbers are optional.

14. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).

### Pin Configuration

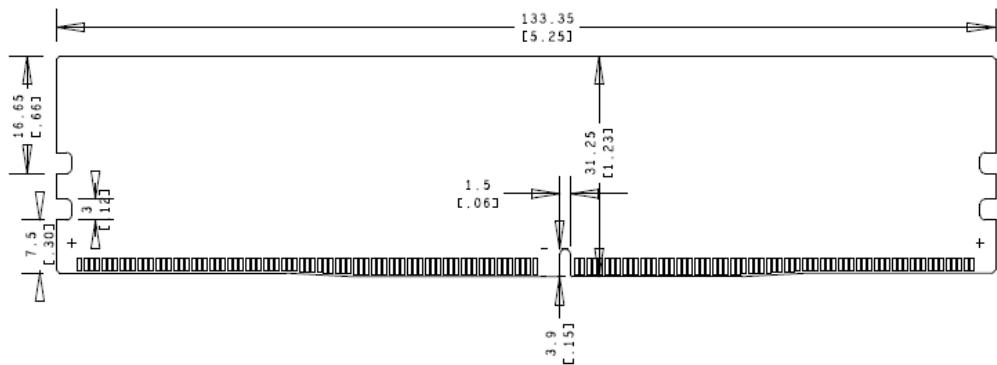
Front Side						Back Side					
1	12V,NC	37	V <sub>SS</sub>	73	V <sub>DD</sub>	109	V <sub>SS</sub>	145	12V,NC	181	DQ29
2	V <sub>SS</sub>	38	DQ24	74	CK0_t	110	DM5_n, DBI5_n	146	V <sub>REFCA</sub>	182	V <sub>SS</sub>
3	DQ4	39	V <sub>SS</sub>	75	CK0_c	111	NC	147	V <sub>SS</sub>	183	DQ25
4	V <sub>SS</sub>	40	DM3_n, DBI3_n	76	V <sub>DD</sub>	112	V <sub>SS</sub>	148	DQ5	184	V <sub>SS</sub>
5	DQ0	41	NC	77	V <sub>TT</sub>	113	DQ46	149	V <sub>SS</sub>	185	DQS3_c
6	V <sub>SS</sub>	42	V <sub>SS</sub>	78	EVENT_n	114	V <sub>SS</sub>	150	DQ1	186	DQS3_t
7	DM0_n, DBI0_n	43	DQ30	79	A0	115	DQ42	151	V <sub>SS</sub>	187	V <sub>SS</sub>
8	NC	44	V <sub>SS</sub>	80	V <sub>DD</sub>	116	V <sub>SS</sub>	152	DQS0_t	188	DQ31
9	V <sub>SS</sub>	45	DQ26	81	BA0	117	DQ52	153	DQS0_c	189	V <sub>SS</sub>
10	DQ6	46	V <sub>SS</sub>	82	RAS_n / A16	118	V <sub>SS</sub>	154	V <sub>SS</sub>	190	DQ27
11	V <sub>SS</sub>	47	CB4,NC	83	V <sub>DD</sub>	119	DQ48	155	DQ7	191	V <sub>SS</sub>
12	DQ2	48	V <sub>SS</sub>	84	CS0_n	120	V <sub>SS</sub>	156	V <sub>SS</sub>	192	CB5,NC
13	V <sub>SS</sub>	49	CB0,NC	85	V <sub>DD</sub>	121	DM6_n, DBI6_n	157	DQ3	193	V <sub>SS</sub>
14	DQ12	50	V <sub>SS</sub>	86	CAS_n / A15	122	NC	158	V <sub>SS</sub>	194	CB1,NC
15	V <sub>SS</sub>	51	NC	87	ODT0	123	V <sub>SS</sub>	159	DQ13	195	V <sub>SS</sub>
16	DQ8	52	NC	88	V <sub>DD</sub>	124	DQ54	160	V <sub>SS</sub>	196	DQS8_c
17	V <sub>SS</sub>	53	V <sub>SS</sub>	89	CS1_n	125	V <sub>SS</sub>	161	DQ9	197	DQS8_t
18	DM1_n, DBI1_n	54	CB6,NC	90	V <sub>DD</sub>	126	DQ50	162	V <sub>SS</sub>	198	V <sub>SS</sub>
19	NC	55	V <sub>SS</sub>	91	ODT1	127	V <sub>SS</sub>	163	DQS1_c	199	CB7,NC
20	V <sub>SS</sub>	56	CB2,NC	92	V <sub>DD</sub>	128	DQ60	164	DQS1_t	200	V <sub>SS</sub>
21	DQ14	57	V <sub>SS</sub>	93	CS2_n,C0,NC	129	V <sub>SS</sub>	165	V <sub>SS</sub>	201	CB3,NC
22	V <sub>SS</sub>	58	RESET_n	94	V <sub>SS</sub>	130	DQ56	166	DQ15	202	V <sub>SS</sub>
23	DQ10	59	V <sub>DD</sub>	95	DQ36	131	V <sub>SS</sub>	167	V <sub>SS</sub>	203	CKE1
24	V <sub>SS</sub>	60	CKE0	96	V <sub>SS</sub>	132	DM7_n, DBI7_n	168	DQ11	204	V <sub>DD</sub>
25	DQ20	61	V <sub>DD</sub>	97	DQ32	133	NC	169	V <sub>SS</sub>	205	RFU
26	V <sub>SS</sub>	62	ACT_n	98	V <sub>SS</sub>	134	V <sub>SS</sub>	170	DQ21	206	V <sub>DD</sub>
27	DQ16	63	BG0	99	DM4_n, DBI4_n	135	DQ62	171	V <sub>SS</sub>	207	BG1
28	V <sub>SS</sub>	64	V <sub>DD</sub>	100	NC	136	V <sub>SS</sub>	172	DQ17	208	ALERT_n
29	DM2_n, DBI2_n	65	A12 / BC_n	101	V <sub>SS</sub>	137	DQ58	173	V <sub>SS</sub>	209	V <sub>DD</sub>
30	NC	66	A9	102	DQ38	138	V <sub>SS</sub>	174	DQS2_c	210	A11
31	V <sub>SS</sub>	67	V <sub>DD</sub>	103	V <sub>SS</sub>	139	SA0	175	DQS2_t	211	A7
32	DQ22	68	A8	104	DQ34	140	SA1	176	V <sub>SS</sub>	212	V <sub>DD</sub>
33	V <sub>SS</sub>	69	A6	105	V <sub>SS</sub>	141	SCL	177	DQ23	213	A5
34	DQ18	70	V <sub>DD</sub>	106	DQ44	142	V <sub>PP</sub>	178	V <sub>SS</sub>	214	A4
35	V <sub>SS</sub>	71	A3	107	V <sub>SS</sub>	143	V <sub>PP</sub>	179	DQ19	215	V <sub>DD</sub>
36	DQ28	72	A1	108	DQ40	144	RFU	180	V <sub>SS</sub>	216	A2
										252	V <sub>SS</sub>
										288	V <sub>PP</sub>

### PIN DESCRIPTION

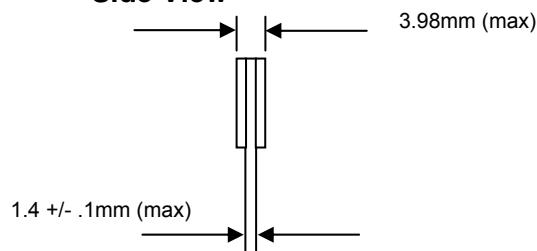
Name	Function
CB[7:0] *	Data Check Bits
DQ[63:0]	Data Bits
DM[7:0]_n, DBI[7:0]_n	Input Data Mask and Data Bus Inversion
DQS[7:0]_t, DQS[7:0]_c	Differential Data Strobes
CK_t[1:0], CK_c[1:0]	Differential Clock Inputs
CKE[1:0]	Clock Enables
CAS_n / A15	Multiplexed: Column Address Strobe or Address 15
RAS_n / A16	Multiplexed: Row Address Strobe or Address 16
CS[1:0]_n, CS[3:2]_n*	Chip Selects
ACT_n	Activate Command Input
WE_n / A14	Multiplexed: Write Enable or Address 14
C[2:0]*	Chip ID Inputs
A[17:0]	Address Inputs
BA[1:0]	Bank Address select Inputs
BG[1:0]	Bank Group select Inputs
ODT[1:0]	On Die Termination Inputs
SA[2:0]	SPD Address
SCL	SPD Clock Input
SDA	SPD Data Input/Output
EVENT_n	Temperature Sensing
RESET_n	Reset for register and DRAMs
PARITY	Parity bit input for Addr/Ctrl
ALERT_n	CRC Error Flag or CMD/Addr Parity Flag Output
A12 / BC_n	Combination Input: Address12/Burst Chop
A10 / AP	Combination Input: Addr10/Auto-precharge
12V*	Optional Power Supply*
V <sub>PP</sub>	Charge Pump Power
V <sub>SS</sub>	Ground
V <sub>DD</sub>	Power
V <sub>DDSPD</sub>	SPD EEPROM Power
V <sub>REFCA</sub>	Reference Voltage for CA
V <sub>TT</sub>	Termination Voltage
NC	No Connection
RFU	Reserved for Future Use

\* Not used

Conforms to MO-309C



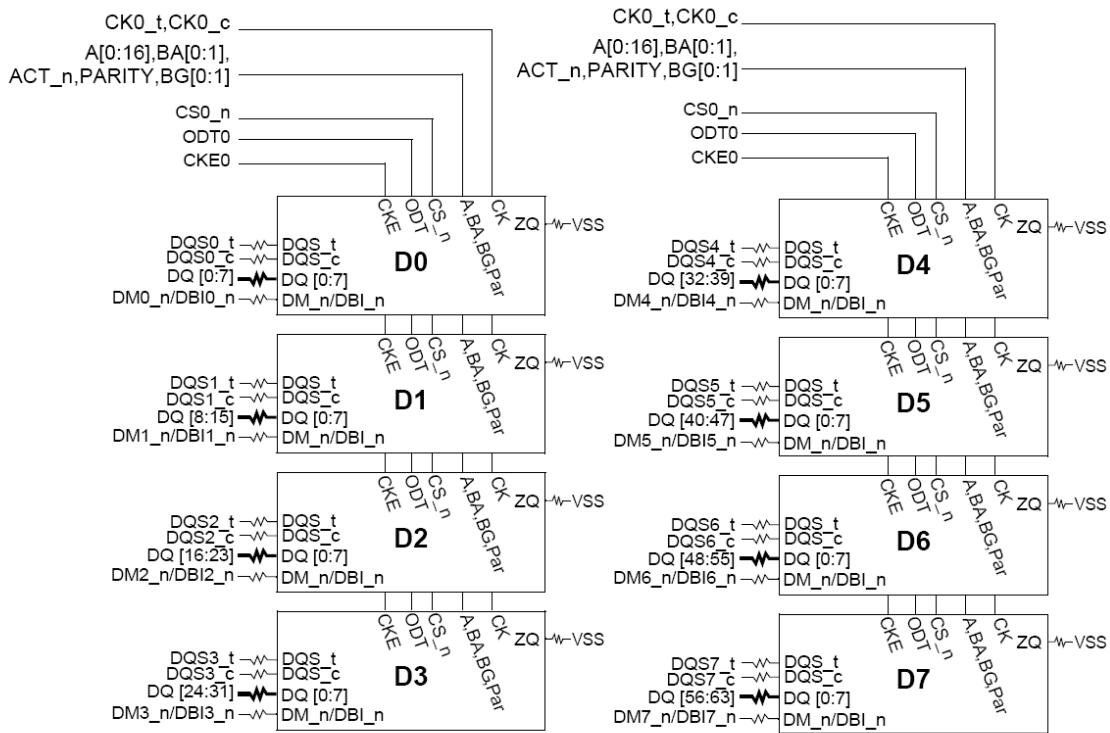
### Side View



### Notes:

1. Tolerances on all dimensions except where otherwise indicated are  $\pm .13$ . Reference JEDEC standard MO-309C.
2. All dimensions are expressed: millimeters [inches]

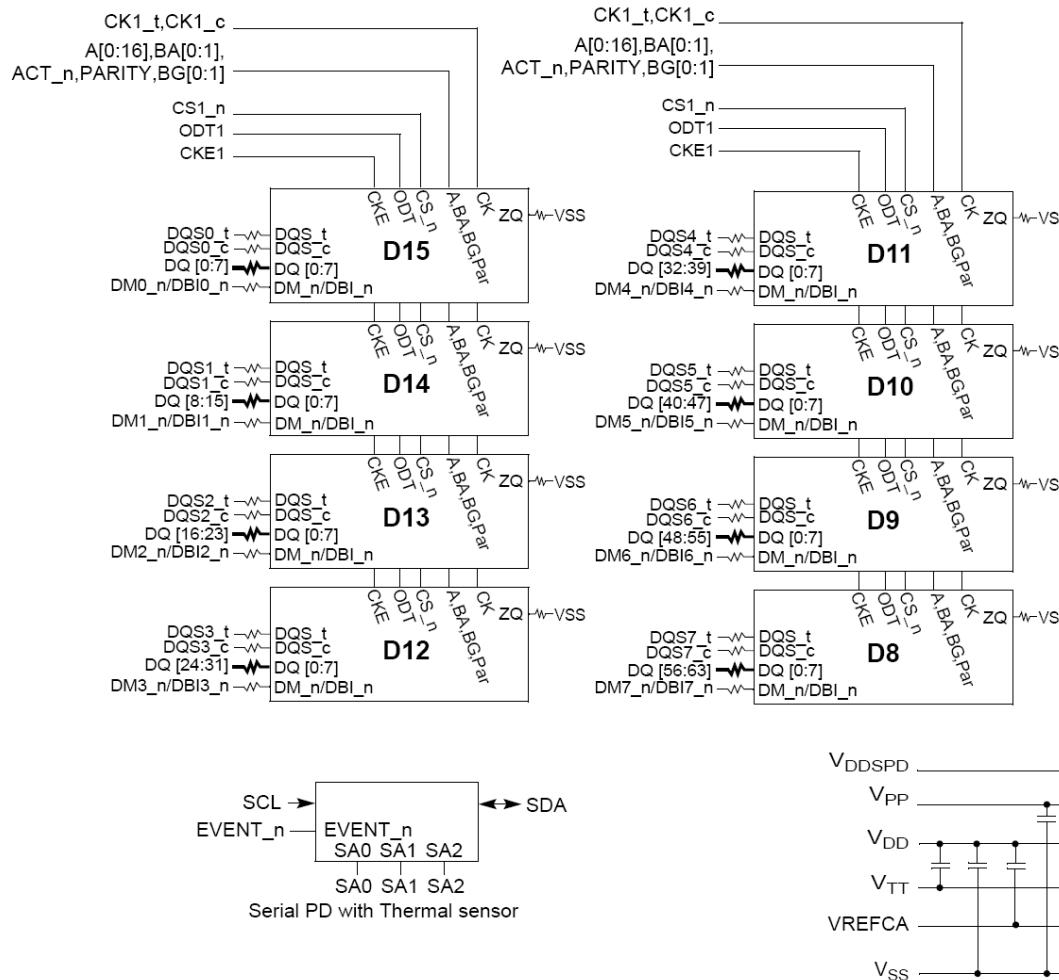
### Functional Diagram (Rank 0)



#### Notes:

- 1: Unless otherwise noted, resistor values are  $15\Omega \pm 5\%$ .
- 2: ZQ resistors are  $240\Omega \pm 1\%$ . For all other resistor values refer to the appropriate wiring diagram.

### Functional Diagram (Rank 1)



#### Notes:

- 1: Unless otherwise noted, resistor values are  $15\Omega \pm 5\%$ .
- 2: ZQ resistors are  $240\Omega \pm 1\%$ . For all other resistor values refer to the appropriate wiring diagram.
- 3: For Rank 1 the DQ resistors are shown for simplicity but are the same physical components as shown on Rank 0.
- 4: EVENT\_n is wired on this design. A standalone SPD may be used as well. No wiring changes are required.



# DTM68104B

8GB - 288-Pin 2Rx8 Unbuffered Non-ECC DDR4 DIMM

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